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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/711,866	11/13/2000	Gerald Sellmair	GR 99 P 5223	8585

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/711,866	SELLMAIR, GERALD	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL OFFICE ACTION

1. This office action is in response to Applicants' **Amendment** of 14 April *2004*.

1.1 Claims 1 and 10 are amended. Claims 1-27 remain pending.

1.2 The objections and rejections of record are withdrawn in response to Applicants' amendment.

Response to Arguments

2. Applicants' arguments of 14 April *2004* are persuasive only to the extent that the feature/step of the simultaneous checking is not specifically described in detail by the prior art of record. Said feature/step is clarified and is further supported by newly found reference in Fig. 7: block 49 of **Bosse** (U.S. Patent No. 4,639,915), as follows.

Claim Rejections - 35 USC § 103

3.1 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.2 **Claims 1-27** are rejected under 35 U.S.C. 103 (a) as unpatentable over NOSE (US Patent No. 6,202,180; Filed: June 15, 1998) in view of **Bosse** (U.S. Patent No. 4,639,915).

As per Claims 1-27, Nose substantially discloses, in Fig. 1-32, an equivalent memory device or means with means for providing plural memory cells and comparator means (and related activation and deactivation thereof e.g. timing input from Block 37 to Block 40 in Fig. 30, col. 12 lines 5-50) to check and match address inputs with reference addresses to effect memory testing including testing and operation mode setting means (Figs. 19-20), means to parallel address (Fig. 21) comparing means, means to permanently replace/repair (Fig. 30 and col. 1 line 22 via fuse or permanent means) defective cells with spare cells or otherwise via

appropriate spare memory cell address substitution means (and related permanent de/activation thereof via fusing, etc.), e.g., Fig. 8 and related description, e.g., *"As shown in FIG. 8, an address signal is supplied via the address comparator 15 from the address input terminal IN to the main memory 16 of a memory cell array which constitutes a memory section. To the memory circuit 13, the address (specified address) regarded as the faulty address based on the result of testing is inputted from the self test circuit 14. The circuit of FIG. 8 is constituted as follow. In the case that the address signal is coincident with the address stored in the memory circuit 13, the spare memory is activated, stores a data corresponding to the address stored in the memory circuit 13 and outputs without conversion of the address. In the circuit of FIG. 8, the selector 18 controlled by the output of the address comparator 15 selects one of the outputs of the main memory 16 and the spare memory 17. FIG. 9 shows a circuit in which spare use (enable)/spare non-use (disable) signal is added and the selector 18 of FIG. 8 is omitted."*

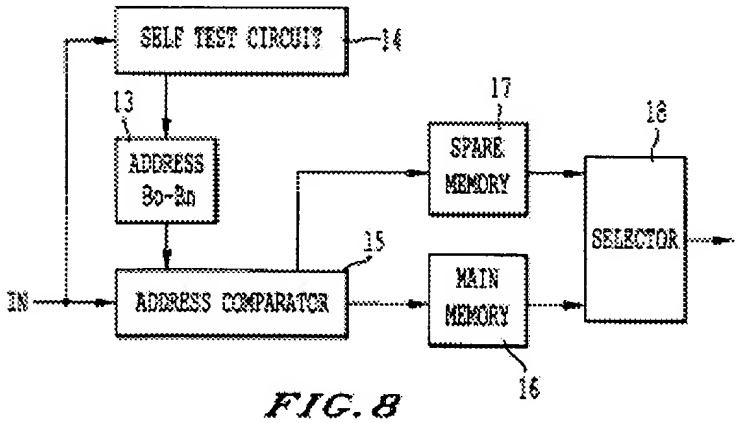

FIG. 8

Nose also discloses "FIG. 10 [which] is a circuit block diagram of a memory circuit including an address exchanging circuit which relieves errors of the memory. The self test circuit 14 operates at the time of power-on and the like. The address, the writing data and the expected value are supplied to the self test circuit 14, and operations of all memory addresses are checked.

The address which is found to be faulty as a result of testing is stored in the memory circuit 13. In the case being disable to repair data by spare memory 17, decided to be fault, a spare-over flag is stored in the memory circuit 13, with the address which is found to be faulty. Simultaneously, a flag showing it is capable of exchanging data between spare memory and main memory, per an address is stored in the memory circuit 19. When the address exchanging circuit of FIG. 10 is actually used, the address data B0 to Bn of the memory circuit 13 is compared with the address data inputted from the address input IN. When both are coincide with each other, and the spare-over flag is activated, the address data C0 to Cn of the memory circuit 19 is used as the address."

NOSE does not explicitly teach of **the simultaneous checking by comparator means.** NOSE, does however, suggest **simultaneous** data or flag comparison means and means to effect simultaneous compares or detections in Figs. 28-29 and col. 11 line 50-65 because once a defective cell is found, the defective address of such cell is stored in a faulty register area and subsequent attempts to access such cell determined as defective are prevented and access is translated/mapped to a spare memory based on simultaneous compare means as seen e.g. in Fig. 30: blocks 17, 40 41. Thus some form of compare means concurrence is effected for defective memory addresses and spare memory area in NOSE. **Accordingly**, **Bosse** in an analogous art teaches of simultaneous checking by comparator means e.g. in Fig. 7: numeral 49 and col. 7 line 50.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify NOSE to include therein simultaneous comparison means as taught by **Bosse** because such modification would provide the procedure disclosed in NOSE with a technique whereby "each cell has its own independent compare circuitry so as to make it possible to match incoming fault address and allow for auto-assignment of spare memory." {See **Bosse,** col. 7 line 53-col. 8 line 67.}

Conclusion

4.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4.2 Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5.3 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
4/21/04